5 Attempt any **two** parts of the following : **5×2=10**

(a) Compare the merits and demerits of open collector and totem pole configuration of TTL logic family.

(b) Describe the following characteristic of logic families :

(1) Fan in

(2) Fan out

(3) Figure of merit

(4) propagation delay

(5) Noise margin.

(c) Write the short notes on any two following :

(1) Ring counter

(2) Mode N counter

(3) RAM.

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Paper ID and Roll No. to be filled in your Answer Book

Roll No.

B. Tech.

(SEM. III) (ODD SEM.) (REG. & BACK) EXAMINATION, 2012-13

DIGITAL ELECTRONICS

Time : **2** Hours] [Total Marks : **50**

Note : *Attempt ALL the questions. Assume suitable data if necessary.*

1 Attempt any **four** parts of the following : **2.5×4=10**

(a) Multiply the following number without converting to decimal: $(367)_8$ and $(715)_8$.

(b) The state of a 12 bit register is 010110010111. What is its content if it represents three decimal digits in (a) BCD (b) Excess-3 code (c) 2421 code.

(c) Design a combinational circuit that multiplies two 2-bit number al a0 and b1 b0 to produce a 4-bit product. Implement it using AND gates and half adders.

(d) What are the universal gates ? And convert NAND gate to Ex-OR gate.

(e) Derive the PLA program table for a combinational circuit that squares a three bit number. Minimize the number of product terms.

(f) Simplify the following Boolean function using five variable k-map and implement using NAND gates only.

F = A'B'CE' + A'B'C'D' + B'CD' + CDE' + BDE'

2 Attempt any **four** parts of the following : **2.5×4=10**

(a) An 8×1 Mux has input a, b and c connected to the selection input S2, S1 and S0 respectively. The data inputs IO through I7 are as follows.

I1 = I2 = I7 = 0; I3 = I5 = 1; I0 = I4 = D and I6 = D'. Determine the Boolean function that the MUX implements.

(b) Design a 4×2 priority encoder.

(c) Convert the negative edge triggered J-K flip flop to SR flip flop to T flip flop.

(d) A JN flip flop has two inputs J and N. Inputs J behaves like the J input of a JK flip flop and input N behaves like the complement of the K input of a JK flip flop that is N=K' .

(1) Tabulate the characteristic table of the flip flop

(2) Tabulate the excitation table of the flip flop.

(3) Show that by connecting the two inputs together, one can obtain a D flip flop.

(e) Discuss about PAL.

(f) Explain the ring counter.

3 Attempt any TWO parts of the following : **5×2=10**

(a) Design a counter with following repeated binary sequence 0, 1, 3, 7, 6, 4. If your design produce a non self correcting counter, modify the circuit to make it self correcting.

(b) A sequential circuit with the two D flip flop input x and y and one output z is specified by the following next state and output equations:

A(t+1) = xy' + xA

B(t+l) = x'B + xA

Z=B

Draw the logic diagram of the circuit. Derive the state table and state diagram.

(c) Construct a BCD ripple counter using a 4-bit binary ripple counter that can be cleared asynchronously and external NAND gate.

4 Attempt any **two** parts of the following : **5×2=10**

(a) A flip flop has a 10 ns delay from the time its clock pulse input goes from 1 to 0 to the time the output is complemented. What is the maximum delay in a 10 bit ripple counter that uses the flip flop . What is the maximum frequency at which the counter can operate?

(b) The content of a 5-bit register is initially 11010. The register is shifted 4 times to the left with the serial input being 101101. What is the content of the register after each shift.

(c) Discuss about the universal shift register in detail.